WHAT IS CLAIMED IS:

1. A clock switching circuit that switches between asynchronous first and second clocks according to whether an interface cable, having a hot-plug function, is connected or disconnected and comprising:

a first flip-flop group that receives an interface disconnection signal that corresponds to the disconnection or connection of the interface cable in response to said first clock, wherein when the interface cable is disconnected, the final-stage flip-flop thereof outputs a first selection signal through the first clock edges whose number is the stage number of the first flip-flop group, and when said interface cable is connected, the final-stage flip-flop outputs a first no-selection signal through one first clock edge, said first flip-flop group outputting said first clock in response to said first selection signal, and prohibitting output of said first clock in response to said first no-selection signal;

a second flip-flop group that receives said interface disconnection signal in response to said second clock, wherein when said interface cable is connected, the final-stage flip-flop thereof outputs a second selection signal through the second clock edges whose number is the stage number of the second flip-flop group, and when said interface cable is disconnected, the final-stage flip-flop outputs a second no-selection signal through

one second clock edge, said second flip-flop group outputting said second clock in response to said second selection signal, and prohibiting output of said second clock in response to said second no-selection signal; and

where the number of stages of said second flip-flop group is greater than the that of said first flip-flop group according to the relationship between the frequency of said first and second clocks.

2. The clock switching circuit of claim 1 wherein; said second clock is supplied from a PLL circuit that generates said second clock from said first clock, and when said interface cable is connected, operation of said PLL circuit starts in response to said interface disconnection signal, and said interface disconnection signal is received by said second flip-flop group after a set time therefrom.

3. The clock switching circuit of claim 2 wherein; when said interface cable is disconnected, operation of said PLL circuit stops in response to said interface disconnection signal.

4. The clock switching circuit of claim 1 wherein; the number of stages of said second flip-flop group is capable of being changed according to the operating

clock frequency of said interface cable to be connected.